1.5A DDR Memory Termination Regulator

NCP51198, NCV51198

The NCP/NCV51198 is a simple, cost−effective, high−speed linear regulator designed to generate the V_{TT} termination voltage rail for DDR−I, DDR−II and DDR−III memory. The regulator is capable of actively sourcing or sinking up to ±1.5 A for DDR−I, or up to ±0.5 A for DDR−II /−III while regulating the output voltage to within ±30 mV.

The output termination voltage is tightly regulated to track V_{TT} = (V_{DDQ} / 2) over the entire current range.

The NCP/NCV51198 incorporates a high−speed differential amplifier to provide ultra−fast response to line and load transients. Other features include extremely low initial offset voltage, excellent load regulation, source/sink soft−start and on−chip thermal shut−down protection.

The NCP/NCV51198 features the power−saving Suspend To Ram (STR) function which will tri−state the regulator output and lower the quiescent current drawn when the /SS pin is pulled low.

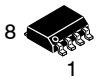
The NCP/NCV51198 is available in a SOIC−8 Exposed Pad package.

Features

- Generate DDR Memory Termination Voltage (V_{TT})
- For DDR−I, DDR−II, DDR−III Source / Sink Currents
- Supports DDR−I to ±1.5 A, DDR−II to ±0.5 A (peak)
- Integrated Power MOSFETs with Thermal Protection
- Stable with 10 μF Ceramic V_{TT} Capacitor
- High Accuracy Output Voltage at Full−Load
- Minimal External Component Count
- Shutdown for Standby or Suspend to RAM (STR) mode
- Built−in Soft Start
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

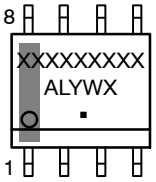
Appications

- Desktop PC's, Notebooks, and Workstations
- Graphics Card DDR Memory Termination
- Set Top Boxes, Digital TV's, Printers
- Embedded Systems
- Active Bus Termination



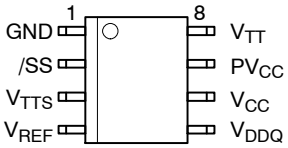
SOIC8−NB EP
PD SUFFIX
CASE 751BU

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTION



SOIC−8 EP

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 8 of this data sheet.

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1.5 A, DDR–I /–II /–III TERMINATION REGULATOR

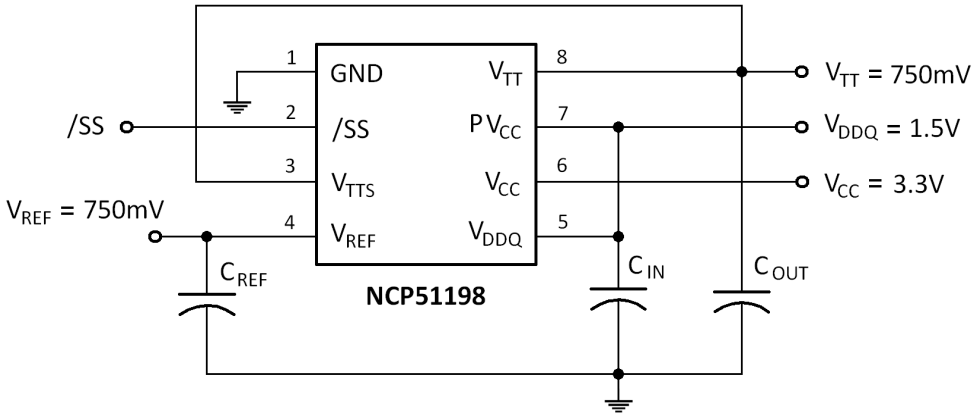


Figure 1. Typical Application Schematic

PIN FUNCTION DESCRIPTION – NCP51198

Pin Number SO8–EP	Pin Name	Pin Function
1	GND	Common Ground.
2	/SS	Suspend Shutdown supports Suspend To RAM function. CMOS compatible input sets V_{TT} output to high impedance state. Logic HI = Enable, Logic LO = Shutdown.
3	V_{TTS}	V_{TTS} is the V_{TT} sense input.
4	V_{REF}	V_{REF} is an output pin that provides the buffered output of the internal reference voltage equal to half of V_{DDQ}. Two resistors dividing down the V_{DDQ} voltage on the pin to create the regulated output voltage.
5	V_{DDQ}	The V_{DDQ} pin is an input pin for creating the internal reference voltage to regulate V_{TT}. The V_{DDQ} voltage is connected to an internal resistor divider. The central tap of resistor divider (V_{DDQ} /2) is connected to the internal voltage buffer, which output is connected to V_{REF} pin and the non–inverting input of the error amplifier as the reference voltage.
6	V_{CC}	Power for the analog control circuitry.
7	PV_{CC}	The PV_{CC} pin provides the rail voltage from where the V_{TT} pin draws load current. There is a limitation between V_{CC} and PV_{CC}. The PV_{CC} voltage must be less or equal to the V_{CC} voltage to ensure the correct output voltage regulation. The V_{TT} source current capability is dependent on PV_{CC} voltage. The higher the voltage on PV_{CC}, the higher the source current.
8	V_{TT}	Regulator output voltage capable of sinking and sourcing current while regulating the output rail.
	THERMAL PAD	Pad for thermal connection. The exposed pad must be connected to the ground plane using multiple vias for maximum power dissipation performance.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC}, PV_{CC} ,V_{DDQ}, /SS to GND (Note 1)		−0.3 to +6	V
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Thermal Characteristics, SO8−EP Thermal Resistance, Junction−to−Air Power Rating at 25°C ambient = 2.3 W, derate 23 mW/°C	$R_{\theta JA}$	43	°C/W
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	150	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. No pin to exceed V_{CC}. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following method:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Bias Supply Voltage	V_{CC}	2.2 to 5.5	V
Input Voltage	PV_{CC}	1.35 to 2.5	V
Reference Input Voltage	V_{DDQ}	1.35 to 2.7	V

ELECTRICAL CHARACTERISTICS

−40°C ≤ T_J ≤ 125°C; V_{CC} = PV_{CC} = V_{DDQ} = 2.5 V; unless otherwise noted. Typical values are at T_J = +25°C

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Reference Voltage (DDR I) I_{REF} = 0 mA (unloaded)	PV_{CC} = V_{DDQ} = 2.3 V = 2.5 V = 2.7 V	V_{REF} (DDR−I)	1.125 1.225 1.325	1.151 1.251 1.351	1.175 1.275 1.375	V
Reference Voltage (DDR II) I_{REF} = 0 mA (unloaded)	PV_{CC} = V_{DDQ} = 1.7 V = 1.8 V = 1.9 V	V_{REF} (DDR−II)	0.830 0.880 0.925	0.851 0.901 0.951	0.880 0.930 0.975	V
Reference Voltage (DDR III) I_{REF} = 0 mA (unloaded)	PV_{CC} = V_{DDQ} = 1.35 V = 1.5 V = 1.6 V	V_{REF} (DDR−III)	0.660 0.735 0.785	0.676 0.751 0.801	0.695 0.770 0.820	V
V_{REF} − Output Impedance	I_{REF} = −30 μA to +30 μA	Z_{REF}		2.5		kΩ
V_{TT} Output Voltage (DDR−I)	I_{OUT} = 0 A PV_{CC} = V_{DDQ} = 2.3 V PV_{CC} = V_{DDQ} = 2.5 V PV_{CC} = V_{DDQ} = 2.7 V	V_{TT} (DDR−I)	− 1.112 1.202 1.312	− 1.150 1.250 1.350	− 1.182 1.282 1.382	V
	I_{OUT} = +1.5 A PV_{CC} = V_{DDQ} = 2.3V PV_{CC} = V_{DDQ} = 2.5V PV_{CC} = V_{DDQ} = 2.7V	V_{TT} (DDR−I)	− 1.115 1.215 1.315	− 1.150 1.250 1.350	− 1.185 1.285 1.385	
	I_{OUT} = −1.5 A PV_{CC} = V_{DDQ} = 2.3V PV_{CC} = V_{DDQ} = 2.5V PV_{CC} = V_{DDQ} = 2.7V	V_{TT} (DDR−I)	− 1.117 1.217 1.317	− 1.150 1.250 1.350	− 1.182 1.282 1.382	

ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 125°C$; $V_{CC} = PV_{CC} = V_{DDQ} = 2.5$ V; unless otherwise noted. Typical values are at $T_J = +25°C$

Parameter	Condition	Symbol	Min	Typ	Max	Unit
V_{TT} Output Voltage (DDR−II)	I_{OUT} = 0 A $PV_{CC} = V_{DDQ}$ = 1.7 V $PV_{CC} = V_{DDQ}$ = 1.8 V $PV_{CC} = V_{DDQ}$ = 1.9 V	V_{TT} (DDR−II)	– 0.816 0.866 0.916	– 0.850 0.900 0.950	– 0.881 0.931 0.981	V
	I_{OUT} = +0.5 A $PV_{CC} = V_{DDQ}$ = 1.7 V $PV_{CC} = V_{DDQ}$ = 1.8 V $PV_{CC} = V_{DDQ}$ = 1.9 V	V_{TT} (DDR−II)	– 0.815 0.863 0.914	– 0.851 0.900 0.950	– 0.885 0.933 0.984	
	I_{OUT} = −0.5 A $PV_{CC} = V_{DDQ}$ = 1.7 V $PV_{CC} = V_{DDQ}$ = 1.8 V $PV_{CC} = V_{DDQ}$ = 1.9 V	V_{TT} (DDR−II)	– 0.814 0.862 0.913	– 0.850 0.900 0.950	– 0.884 0.932 0.983	
V_{TT} Output Voltage (DDR−III)	I_{OUT} = 0 A $PV_{CC} = V_{DDQ}$ = 1.35 V $PV_{CC} = V_{DDQ}$ = 1.5 V $PV_{CC} = V_{DDQ}$ = 1.6 V	V_{TT} (DDR−III)	– 0.650 0.725 0.775	– 0.675 0.750 0.800	– 0.700 0.775 0.825	V
	I_{OUT} = +0.2 A, $PV_{CC} = V_{DDQ}$ = 1.35 V I_{OUT} = −0.2 A, $PV_{CC} = V_{DDQ}$ = 1.35 V	V_{TT} (DDR−III)	– 0.649 – 0.640	– 0.675 – 0.675	– 0.700 – 0.700	
	I_{OUT} = +0.4 A, $PV_{CC} = V_{DDQ}$ = 1.5 V I_{OUT} = −0.4 A, $PV_{CC} = V_{DDQ}$ = 1.5 V	V_{TT} (DDR−III)	– 0.722 – 0.725	– 0.751 – 0.750	– 0.776 – 0.774	
	I_{OUT} = +0.5 A, $PV_{CC} = V_{DDQ}$ = 1.6 V I_{OUT} = −0.5 A, $PV_{CC} = V_{DDQ}$ = 1.6 V	V_{TT} (DDR−III)	– 0.773 – 0.775	– 0.801 – 0.800	– 0.827 – 0.824	
V_{TT} Output Offset Voltage	I_{OUT} = ±1.5 A, $PV_{CC} = V_{DDQ}$ = 2.5 V	V_{OS} (DDR−I)	−30	0	+30	mV
	I_{OUT} = ±0.5A, $PV_{CC} = V_{DDQ}$ = 1.8V	V_{OS} (DDR−II)	−30	0	+30	
	I_{OUT} = ±0.5A, $PV_{CC} = V_{DDQ}$ = 1.5V	V_{OS} (DDR−III)	−30	0	+30	
Quiescent Current	I_{OUT} = 0 A	I_Q		380	500	μA
V_{DDQ} Input Impedance		Z_{VDDQ}		100		kΩ
/SS Leakage Current	/SS = 0 V	I_{L_SS}		2	5	μA
Quiescent Current in Suspend Shutdown	/SS = 0 V	I_{Q_SS}		115	150	μA
Suspend Shutdown Threshold		V_{IH}	1.9			V
		V_{IL}			0.8	
V_{TT} leakage Current in Suspend Shutdown	/SS = 0 V, V_{TT} = 1.25 V	I_{L_VTT}		1	10	μA
V_{TTS} Current		I_{TTS}		13		nA
Thermal Shutdown Temperature		T_{SD}		165		°C
Thermal Shutdown Hysteresis		T_{SH}		10		°C

TYPICAL PERFORMANCE CHARACTERISTICS

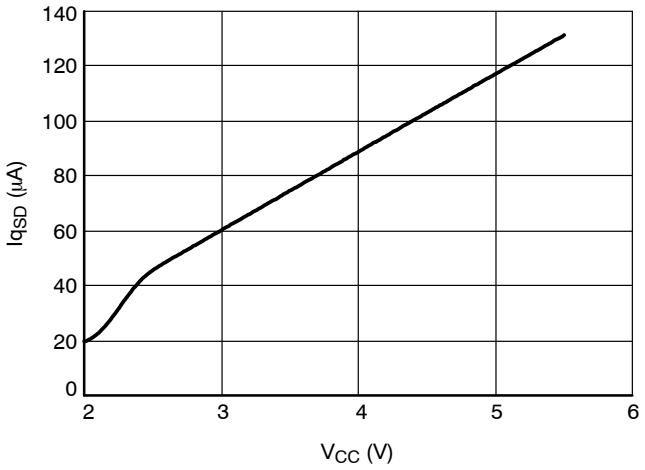


Figure 2. Iq_{SD} vs. V_{CC}

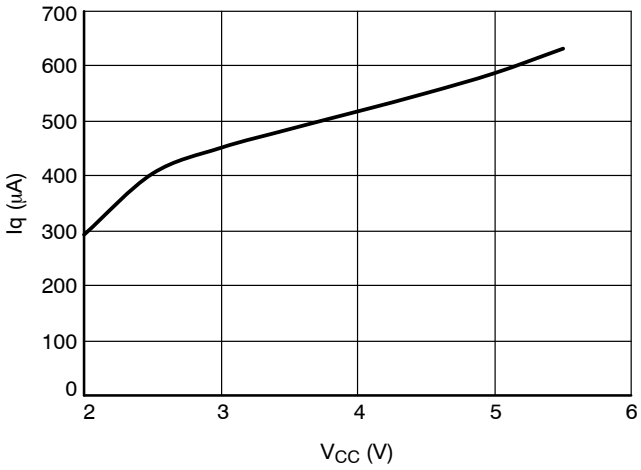


Figure 3. Iq vs. V_{CC}

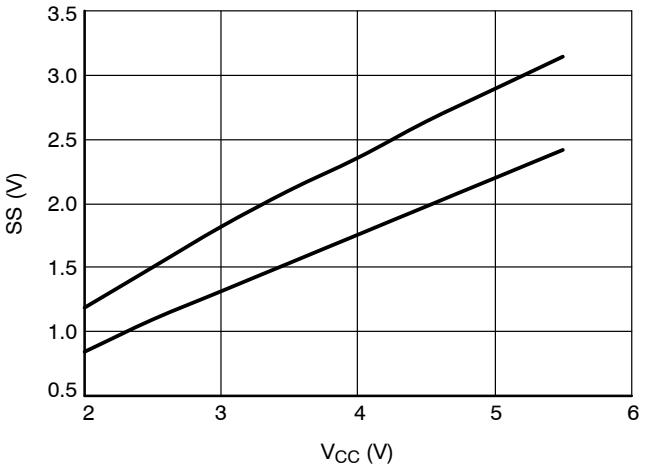


Figure 4. V_{IH} and V_{IL}

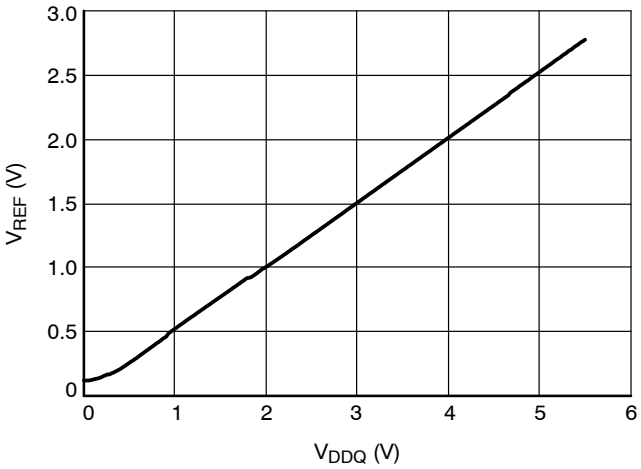


Figure 5. V_{REF} vs. V_{DDQ}

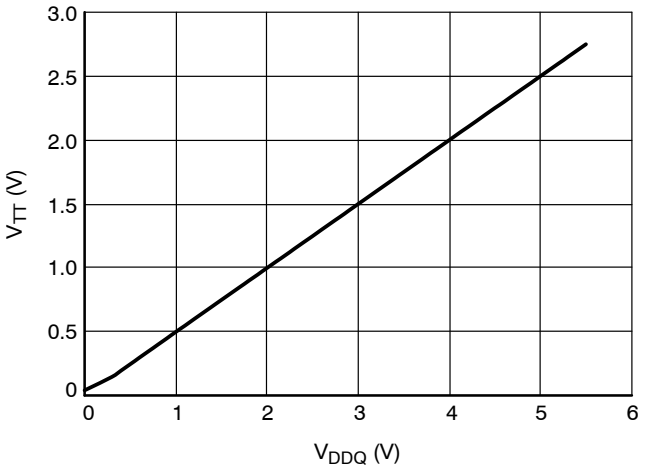


Figure 6. V_{TT} vs. V_{DDQ}

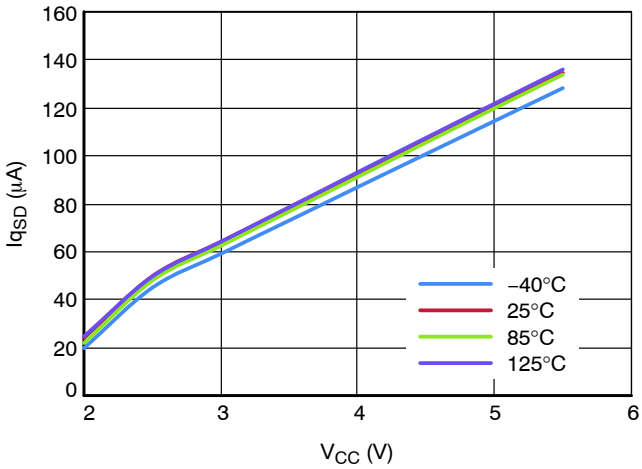


Figure 7. Iq_{SD} vs. V_{CC} over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

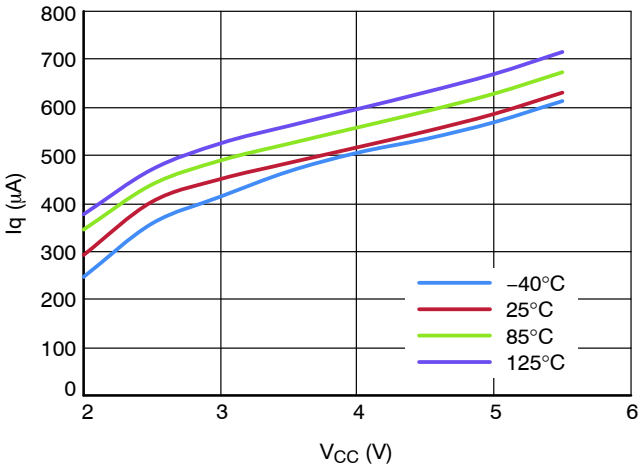


Figure 8. Iq vs. V_{CC} over Temperature

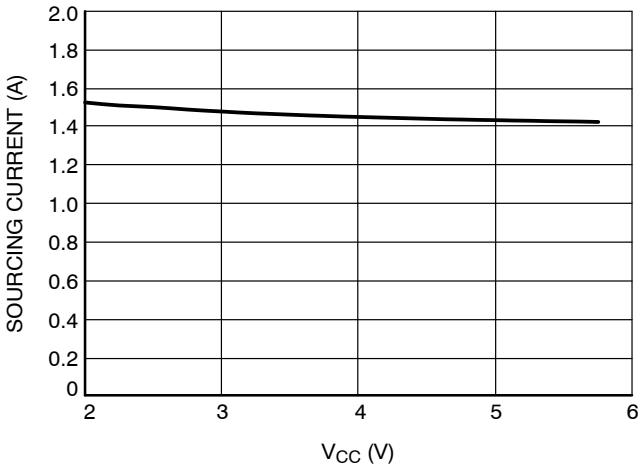


Figure 9. Maximum Sourcing Current vs. V_{CC} (V_{DDQ} = PV_{CC} = 1.8 V)

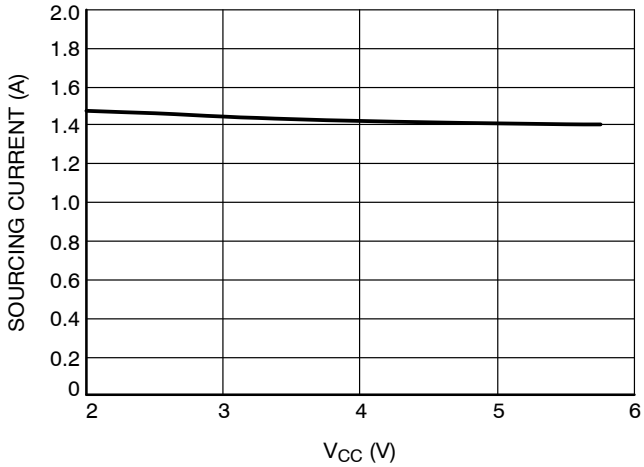


Figure 10. Maximum Sourcing Current vs. V_{CC} (V_{DDQ} = 2.5 V, PV_{CC} = 1.8 V

APPLICATIONS INFORMATION

General

The NCP/NCV51198 is a bus termination, linear regulator designed to meet the JEDEC requirements for DDR−I, DDR−II and DDR−III memory termination. The NCP/NCV51198 is capable of sourcing and sinking current while accurately tracking and regulating the V_{TT} output voltage equal to (V_{DDQ} / 2). The output stage has been designed to maintain excellent load regulation and preventing shoot−through. The NCP/NCV51198 uses two distinct power rails to separate the analog circuitry from the power output stage and decrease internal power dissipation.

Supply Voltage Inputs

For added flexibility, separate input pins (V_{CC} and PV_{CC}) are provided for each required supply input. V_{CC} is used to supply all the internal control circuitry and PV_{CC} is used exclusively to provide the rail voltage for the output stage used to create V_{TT}. These pins have the capability to work off separate supplies with the condition that V_{CC} is always greater than or equal to PV_{CC}, and should always be used with either a 1.8 V or 2.5 V rail. If the junction temperature exceeds the thermal shutdown threshold, the part will enter a shutdown state identical to the manual shutdown where V_{TT} is tri−stated and V_{REF} remains active. Lower voltage rails, such as 1.5 V can be used but will reduce the maximum available output current.

Generation of Internal Voltage Reference

V_{DDQ} is the input used to create the internal reference voltage for regulating V_{TT}. The reference voltage is generated from a resistor divider of two internal 50 kΩ resistors. This guarantees that V_{TT} will precisely track (V_{DDQ} / 2). The optimal implementation of the V_{DDQ} input pin is as a remote sense. This can be achieved by connecting V_{DDQ} directly to the 1.8 V rail at the DIMM memory module instead of connecting it to PV_{CC}. This ensures that the reference voltage precisely tracks the DDR memory power rail without introducing a large voltage drop due to power traces. For DDR−II applications the V_{DDQ} input will be 1.8 V, which will create a (V_{DDQ} / 2) = 0.9 V termination voltage at the V_{TT} output.

V_{REF} provides a buffered output of the internal reference voltage (V_{DDQ} / 2). For improved performance, an output bypass capacitor can be placed, close to the pin, to help reduce any potential stray noise. A ceramic capacitor in the range of 0.01 μF to 0.1 μF is recommended. The V_{REF} output remains active during the shutdown state and thermal shutdown events for the suspend to RAM functionality.

Remote Voltage Feedback Sensing

The purpose of the V_{TTS} sense pin is to provide improved remote load regulation. In most motherboard applications, the termination resistors will connect to V_{TT} in a long plane. If the output voltage was regulated only at the output of the NCP/NCV51198, then any long traces will generate a significant IR drop resulting in a sagging termination voltage at one end of the bus than the other. The V_{TTS} pin can be used to improve performance by connecting it to the middle of the bus. This will provide better power distribution across the entire termination bus. If remote load regulation is not used, then the V_{TTS} pin must still be connected to V_{TT}. Care should be taken when a long V_{TTS} trace is implemented in close proximity to the memory. Noise pickup in the V_{TTS} trace can cause problems with precise regulation of V_{TT}. A small 0.1 μF ceramic capacitor placed next to the V_{TTS} pin can help filter out any high frequency noise and thereby keeping the V_{TT} power rail in spec.

Regulator Shutdown Function

The NCP/NCV51198 contains an active low enable pin (/SS) that can be used for suspend to RAM functionality. In this condition the V_{TT} output will tri−state, with the V_{REF} output remaining active in order to provide a constant reference signal for the memory and chipset. During shutdown, V_{TT} should not be exposed to voltages that exceed PV_{CC}.

With the enable pin asserted low the quiescent current of the NCP/NCV51198 will drop, however the V_{DDQ} input pin will always draw a constant current due to the integrated 100 kΩ impedance used for generating the internal reference. Therefore, to calculate the total power loss in shutdown, both currents need to be considered. The enable pin also has an internal pull−up current. Therefore, to turn the part on, the enable pin can either be connected to V_{CC} or left open.

Termination Voltage Output Regulation

V_{TT} is the regulated output that is used to terminate the bus resistors. It is capable of sourcing and sinking current while regulating the output precisely to V_{DDQ} / 2. The NCP/NCV51198 is designed to handle continuous currents of up to ±1.5 A with excellent load regulation. If a transient is expected to last above the maximum continuous current rating for a significant amount of time, then the bulk output capacitor should be sized large enough to prevent an excessive voltage drop.

Thermal Shutdown with Hysteresis

If the NCP/NCV51198 is to operate in elevated temperatures for long durations, care should be taken to ensure that the maximum operating junction temperature is not exceeded. To guarantee safe operation, the NCP/NCV51198 provides on−chip thermal shutdown protection. When the chip junction temperature exceeds 165°C (typical) the part will shutdown. When the junction temperature falls back to 155°C (typical) the device resumes normal operation. If the junction temperature exceeds the thermal shutdown threshold, V_{TT} will tri−state until the part returns below the temperature hysteresis trip−point.

Table 1. ORDERING INFORMATION

Device	Marking	Package	Shipping †
NCP51198PDR2G	51198	SOIC−8 (Pb-Free)	2500 / Tape & Reel
NCV51198PDR2G*	V51198		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

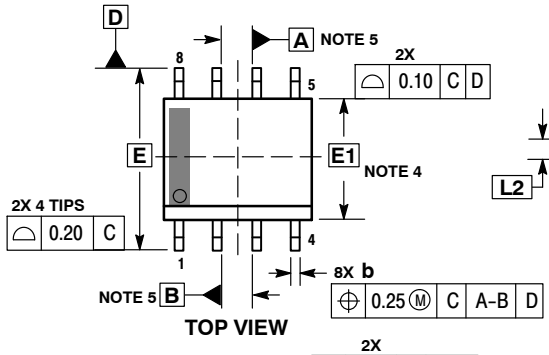
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

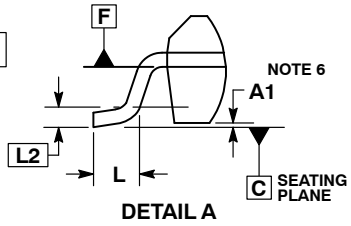
SCALE 1:1

SOIC8−NB EP
CASE 751BU
ISSUE E

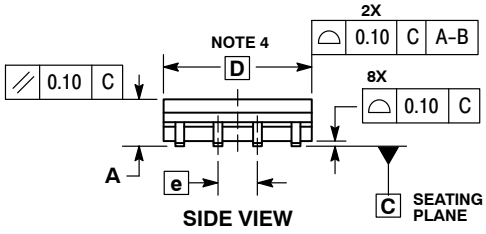
DATE 01 APR 2015



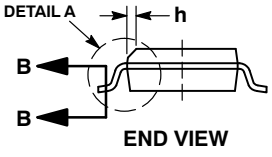
TOP VIEW



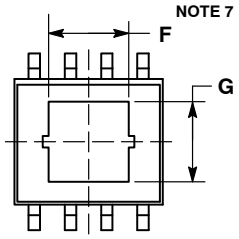
DETAIL A



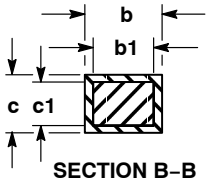
SIDE VIEW



END VIEW



BOTTOM VIEW

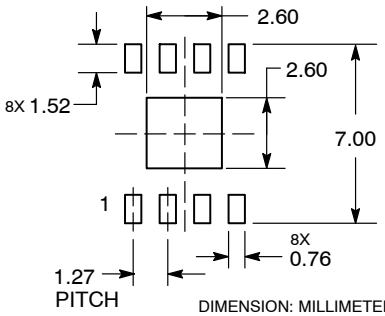


SECTION B−B

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. TAB CONTOUR MAY VARY MINIMALLY TO INCLUDE TOOLING FEATURES.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
F	1.55	2.39
G	1.55	2.39
h	0.25	0.50
L	0.40	1.27
L2	0.25 BSC	

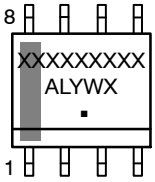
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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